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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 09/900,940 | 07/09/2001 | David N. Pether | 00-339 1496.00116 | 9547 |

24319 7590 07/28/2005

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| EXAMINER | |
|---|---|
| KOSTAK, VICTOR R | |
| **ART UNIT** | **PAPER NUMBER** |
| 2614 | |

DATE MAILED: 07/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/900,940 | PETHER, DAVID N. | |
| | Examiner | Art Unit | |
| | Victor R. Kostak | 2614 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *11 May 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-4,6-8,10-15,17,18 and 21-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,6,8,10-12,17,18,21 and 22* is/are rejected.

7)☒ Claim(s) *7,15 and 23-26* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. Applicant is informed that the Bilbrey reference, previously made of record and applied in a rejection, is again listed on the attached PTOL-892 form because the Office file is missing that original form.

2. It is also noted that applicant added the phrase *"in response to a data request signal"* to independent claims 1 and 13, but not to independent claim 12. The examiner brings that to the attention of the applicant for clarification of it being intentional or inadvertent.

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 6, 8, 10-12, 17, 18 and 22 are now rejected under 35 U.S.C. 103(a) as being unpatentable over Deering.

The graphics processor of Deering (noting particularly Figs. 1, 2, 4 and 5) includes a first circuit (covering elements 50-54) configured to calculate and present an output signal having a first resolution comprising plural output pixels (eventually to postprocessor 70 and ultimately displayed on unit 26), in response to an input signal having a first resolution and respective plural input pixels, and in response to (at least one) control signal (e.g. col. 2 lines 33-51). A second circuit comprises (at least) components 30 and 40-43 configured to generate the control signal(s) in response to (at least one) input parameter (noting again col. 2 lines 40-45), and in response to a previous calculation (i.e. the image processing can be done over and readily altered

if so desired by the operator), wherein the processing on the input signal can include scaling and filtering, plural pixels being combined to generate the output pixels (e.g. col. 11 lines 36-44; col. 5 lines 63-65; col. 21 line 30 and lines 35-61; col. 14 lines 22-24). Register file 142 (in floating point processor 40 detailed in Fig. 4) responds to request signals for passing image data to draw processor 50 (col. 9 line 68 – col. 10 line 4).

Although Deering does not specify that the register stores a scan line at a time, it would have been obvious to one of ordinary skill in the art to transfer data and operate on data in manageable amounts, particularly since graphics data and image data generally are organized in plural lines forming a two-dimensional image unit. Moreover, since his register file comprises 160 32-bit registers (col. 9 lines 53-54), and since draw processor 50 operates on a scan line at a time (col. 10 lines 32-38 and lines 59-63), it would therefore have been obvious to transfer the image data a scan line at a time, thereby meeting claims 1 and 12.

As for claim 13, Deering also points out that unit 30 includes block move capabilities (e.g. col. 4 lines 53-57).

As for claim 4, the scaling involves calculation of the horizontal and vertical components of the output signal since the processing works on one line at a time.

As for claims 6 and 17, since block moving is disclosed, the apparatus (composite circuit shown in Fig. 2) accordingly can process at least one data block.

Regarding claim 8, the draw processor operates on a scan line at a time as noted previously, and passes the processed data to a memory 61.

As for claims 10 and 21, at least two input pixels are blended or interpolated to form one or more output pixels (e.g. col. 11 lines 36-44; col. 5 lines 63-65; col. 21 line 30 and lines 35-61; col. 14 lines 22-24).

As for claim 11, col. 11 lines 36-44 describe scaling of alpha data (as well as col. 21 lines 27-61).

Considering claim 18, block moving is initially done by preprocessor 30, and subsequent image processing is done on a line-by-line basis, as note previously.

As for claim 22, host element 20 (noting fig. 1) can include any type of controller such as a computer processor, multiprocessor, CPU, etc., and is connected to the first and second circuits by bus 28 (col. 3 lines 45-53).

4. Claims 2, 3 and 14 are now rejected under 35 U.S.C. 103(a) as being unpatentable over Deering in view of Hong.

Deering does not describe in extensive detail the specific data transfer logic into or out from register file 142 (noting the general arrangement shown in Fig. 4), thereby suggesting that any suitable logic elements would have been obvious to use.

It would have been obvious to use a multiplexer to output data from the plural component register elements (Deering mentions 160 such elements) to the downstream draw processor, for the clear purpose of limiting hardware connections that involve plural associated data transfer, such as the multiplexer used by Hong in his register file transfer (Fig. 1 elements 130, 142 and 143), the data of Deering accordingly being read out in a controlled manner (element 144).

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

6. Claims 7, 15 and 23-26 appear allowable over the prior art.

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Victor R. Kostak whose telephone number is (571) 272-7348. The examiner can normally be reached on Monday - Friday from 6:30am-3:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John W. Miller can be reached on (571) 272-7353.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

**Any response to this final action should be mailed to:**

Box AF
Commissioner of Patents and Trademarks
P.O. Box 1450
Alexandria, Virginia 22313-1450

**Or faxed to:**

**(571) 273-8300**

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Customer Service Office whose telephone number is (703) 308-HELP.

Victor R. Kostak
Primary Examiner
Art Unit 2614

VRK